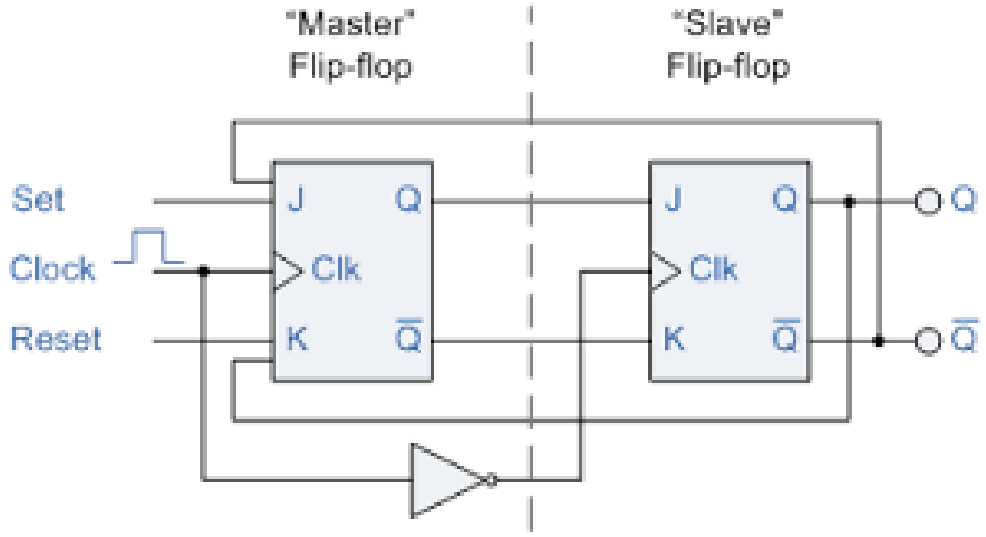
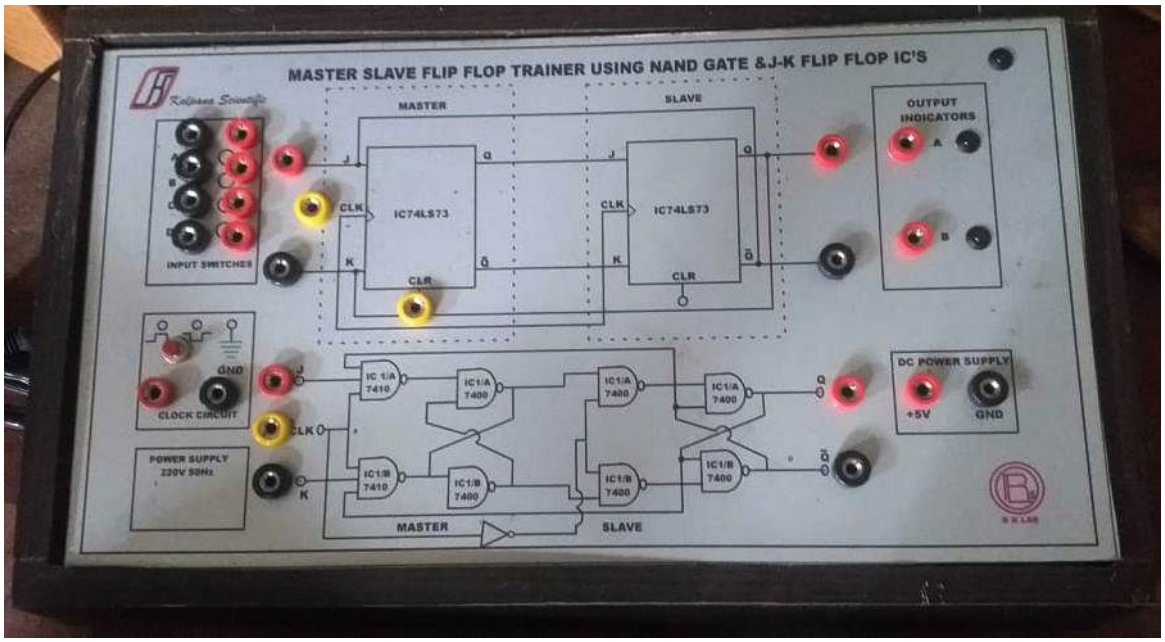
TO DESIGN JK-MS FLIP FLOP USING FLIP FLOP IC





AIM:

To design a JK-MS Flip Flop by using NAND gates as well as Flip Flop IC-7473

APPARATUS USED:

- Flip Flop IC (7473)
  (Upper part of trainer kit)
- Inbuilt Flip Flop using NAND gates
  (Lower part of trainer kit)
- Input digital supply
- Clock pulse generator
- Power Supply (5v / 12v)
- Connecting wires
- Indicator LED's

Single Kit

THEORY:

FLIP FLOPS: Different digital systems need some circuit to store the binary data for some time. Storing of data could be done in different ways. But the basic building blocks used in such memory circuits is a flip flop or a bi-stable circuit. A bi-stable circuit, as the name indicates, possesses two stable states. The circuit can be forced to change from one stable state to the other by an external signal or a trigger. But unless forced, the circuit never changes its state of its own.

There are many types of flip flops like, RS flip flop, JK flip flop & JK-MS flip flop etc.

JK-MS FLIP FLOP: A JK-Master Slave (MS) flip flop consists of two gated or clocked RS flip flops, called as a Master and a Slave. Output of the 2^{nd} flip flop (slave) is fed back to the input of the 1^{st} (master). Clock is directly supplied to

the master, while to the slave it is supplied through an inverter (NOT gate). Thus master can change state when clock goes high, whereas the slave changes its state only when clock goes low.

The basic block diagram & the circuit diagram of a JK-MS flip flop is given by fig.1(a) & fig.1(b) respectively.

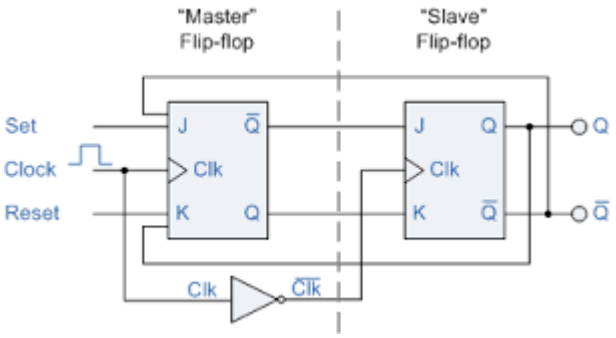


Fig.1(a) Block Diagram of JK-MS flip flop

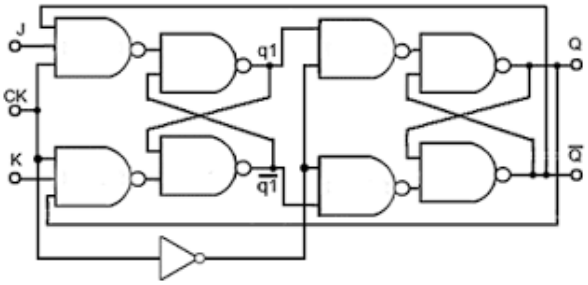


Fig.1(b) Circuit Diagram of JK-MS flip flop

TRUTH TABLE:

Input			Output
CK	**J**	**K**	**Q**
0	X	X	No Change
1	0	0	No Change
1	0	1	0 (RESET)
1	1	0	1 (SET)
1	1	1	Toggle

NB : 1. Here no change of the output means the output is at its initial or previous state.

PIN DESCRIPTION OF IC-7473:

The pin diagram of IC-7473 is given in the fig.2 below,

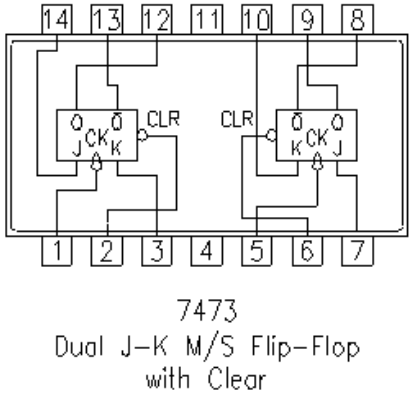


Fig.2 Pin Diagram of IC-7476 (JK-MS)

Pin No.	Details
01	Clock input for the 1st JK flip flop
02	Clear terminal for 1st JK flip flop (for setting up the initial state)
03	K-input for the 1st JK flip flop
04	VCC (Supply Voltage) (+ 5v)
05	Clock input for the 2nd JK flip flop
06	Clear terminal for 2nd JK flip flop (to clear the output)
07	J-input for the 2nd JK flip flop
08	Complementary Output of the 2nd JK flip flop
09	Output of the 2nd JK flip flop
10	K- input for the 2nd JK flip flop
11	Power Supply Ground
12	Output of the 1st JK flip flop
13	Complementary Output of the 1st JK flip flop
14	J-input for the 1st JK flip flop

PROCEDURE:

- Turn on the trainer kit. The power indicator LED at the top right corner of the trainer kit will start to glow.
- The Selector switch provided in between the output terminals of the upper and lower part of the trainer it is to be set to the upper side to select the JK-MS flip flop using IC-7473 to be powered
- Connect the J & K input of the flip flops to the input switches (Input supply) using patch chords and similarly connect the outputs to the output indicators and clock input to the respective clock pulse generator input. Connect the clear terminal to Positive input supply (Red) after clearing the outputs by once touching it to negative input supply for few seconds (Black).
- Now follow the truth table for the successful operation of the JK-MS flip
- Now the Selector switch provided in between the output terminals of the upper and lower part of the trainer it is to be set to the lower side to select the JK-MS flip flop using NAND GATES to be powered
- Connect the J & K input of the flip flops to the input switches (Input supply) using patch chords and similarly connect the outputs to the output indicators and clock input to the respective clock pulse generator input.
- Now follow the truth table for the successful operation of the JK-MS flip flop. Change the inputs (J & K) of the 1st JK flip flop to get the desired output.
- The logic state of the output can be recognized by the LED's connected along it.

OBSERVATION TABLE (Truth Table) :

Input			Output	
CK	**J**	**K**	**Q**	**$\overline{Q}$**